



Low Power VLSI

Dr. Chhavi Saxena

*Associate Professor
Maharana Pratap College of Technology, Gwalior*

It's no secret that power is emerging as the most critical issues in system-on-chip (SoC) design today. Power management is becoming an increasingly urgent problem for almost every category of design, as power density-measured in watts per square millimeter-rises at an alarming rate.

Moving a design from an old technology to a newer one, with smaller design rules, has always been, up to now, an interesting way to lower the power consumption. Indeed, the overall parasitic capacitances are decreased, the available active current per device is higher, and, consequently, the same performance can be achieved with a lower supply voltage. Moving to a new technology generation, however, induces a scale down of the power supply voltage (V_{DD}), the threshold voltage (V_T), and the gate oxide thickness (T_{OX}). Beginning with the $0.18\mu\text{m}$ technologies, it appeared that building a transistor with a good active current (I_{ON}) and a low leakage current (I_{OFF}) was becoming more difficult. Since the advent of CMOS technology, an increased number of transistors per die and greater performance have been the primary driving factors for the semiconductor industry and process technology. The ability to integrate more transistors per die allowed chip manufacturers to put more components of a system into a single package and thus reduce not only just the sizes of the electronic devices we use today but also the cost and delay. The intense competition in the semiconductor industry has forced chip manufacturers pursue these great goals.

However, the increase in the number of devices due to the increase in device density has more than compensated for the decrease in the parasitic capacitance of a single device. In addition to shortened battery life for portable electronics, higher power consumption results in aggravated on-chip temperatures, which can result

in a reduced operating life for the IC. For portable electronics, longer battery life is the most important design constraint.

As a result, low power consumption becomes a crucial requirement for circuits used in portable electronics. In fact, the rapid growth in the demand for portable electronics is one of the major drivers that have forced semiconductor manufacturers to make conscious efforts to reduce power consumption.

Power consumption has emerged as a very significant design parameter, which should be taken into consideration by the designer. Both market forces and process technology have driven power to the forefront of all factors constraining electronic design. The increasing demand for high-performance, battery-operated, system-on-chips (SoC) in communication and computing has shifted the focus from traditional constraints (such as area, performance, cost, and reliability) to power consumption. Just as important, though not so obvious, is the need to reduce power consumption for non-portable systems, such as base stations, where heat dissipation and energy consumption are critical concerns. Today power dissipation is the primary limiting factor. There are four sources of power dissipation in digital CMOS circuits. This is summarized as:

$$P_{average} = P_{switching} + P_{short-circuit} + P_{leakage} + P_{static}$$
$$= \alpha_{0>1} C_1 \cdot V \cdot V_{dd} \cdot f_{clk} + I_{sc} \cdot V_{dd} + I_{leakage} \cdot V_{dd} + I_{static} \cdot V_{dd}$$

$P_{switching}$ represents the switching component of power, where C_1 is load capacitance, f_{clk} is the clock frequency and $\alpha_{0>1}$ is the node transition activity factor. In most cases, the voltage swing, V is the sum of the supply voltage; V_{dd} . $P_{short-circuit}$ is due to the direct path short circuit current, I_{sc} , which at when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. $P_{leakage}$ is due to the leakage current $I_{leakage}$, which can arise from reverse bias diode currents and sub- threshold effects. P_{static} is negligible if the circuit is designed well.

Low-power designs have become ubiquitous in today's world. Designers of consumer and mobile products create aggressive low-power designs to compete on extended battery life. Tethered device designers (e.g., servers and routers) want to reduce cost of ownership. Consumers are also more conscious of "green" design in every area of electronics. Today, low-power designs are so popular that nine of ten new designs implement one or more power management techniques. Meanwhile, the design efforts in managing power are rising due to the

necessity to design for low power as well as for performance and costs. This has ramifications for engineering productivity, as it impacts schedules and risk.

Low-power design of VLSI circuits and systems is very much essential . Of course, what source of power dissipation to be reduced and what type of power profile metric to be considered may vary depending on the applications.